APPLICATION

OF

JAMES D. PARSONS

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ON

BONDED STRUCTURE USING REACTED BOROSILICATE MIXTURE

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BONDED STRUCTURE USING REACTED BOROSILICATE MIXTURE

This application is related to U.S. patent application Serial Nos. 09/316,239 and 09/645,383, filed respectively on May 21, 1999 and August 28, 2000 by the
5   present inventor.

BACKGROUND OF THE INVENTION

Field of the Invention

10   This invention relates to the bonding of ceramic, semiconductor and metallic materials to each other, and more particularly to securing an array of environmental sensors and their associated lead wires to a common substrate.

15

Description of the Related Art

In applications such as the semiconductor and liquid crystal display (LCD) manufacturing industries, it is necessary to sense the absolute value and uniformity of
20   environmental factors, such as temperature, radiation, pressure and gas composition and/or concentration, over a given surface area. To this end a plurality of sensors are disposed on a substrate which has the desired area and is placed in the location where sensing is needed.
25   Each sensor, which is typically pre-calibrated to correlate with the values of the sensed quantity, is connected by lead wires to a remotely located response facility which responds to the sensor output, such as by providing a readout of the sensed environmental

characteristic and/or controlling other elements of the manufacturing process.

In semiconductor and LCD manufacturing, the absolute temperature and temperature uniformity in processing equipment are important parameters in establishing manufacturing yields. Such processing equipment includes furnaces (such as rapid thermal process, tube, belt and tray furnaces), vacuum sputtering and evaporation equipment, chemical vapor deposition reactors, plasma, reactive ion and wet chemical etchers, the application and removal of photo resist and glass for spinners, chill plates, hot plates and strippers, and wafer and plate chucks used for device and integrated circuit (IC) testing.

The thermal sensors are typically type K, R or S thermocouples (TCs) or thin film platinum resistance temperature detectors (TFRTDs). The TC junctions or TFRTDs are typically mounted within respective cavities in the substrate, and secured within the cavities by a bonding material. The bonding material for TCs is commonly a mixture of SiO_2 and Al_2O_3, typically 60wt.% SiO_2 and 40wt.% Al_2O_3. TFRTD sensors typically require two cavities each, one for the sensor itself and the other to strengthen lead wire bonding, with the bonding material for both cavities typically an epoxy.

The electrical lead wires for the sensors are typically sheathed in quartz microtubing segments having a maximum temperature rating of 1100°C, braided silica sleeving having a maximum temperature rating of 1100°C, or Teflon® sleeving having a maximum temperature rating of 250°C. The lead wires extend from their respective sensors

and are commonly bundled together, with the bundling commencing either on or off the substrate.

Cavities are necessary for accurate temperature calibration of TCs because the TC junctions, plus at
5   least about 2.5 cm of lead wire extending from the junction, must be inside the temperature measurement volume for accurate measurements. Cavities are not necessary for accurate temperature calibration of surface sensors such as TFRTDs, since such sensors need only be
10 in intimate contact with an object to provide accurate temperature measurement. However, in the case of TFRTDs, cavities are commonly employed for purposes of mounting stability.

The substrates typically employed for the sensors,
15 including glass, ceramic and semiconductor wafers, are relatively brittle. Furthermore, semiconductor wafers are generally single crystals that are subject to breakage from mechanical intrusion. The provision of cavities in a substrate therefore makes the substrates much more
20 fragile then would otherwise be the case, and reduces their manufacturing yield.

Another problem is that the mechanical bond of the sensor to the substrate is often easy to break. This is because the bonding materials presently employed can only
25 bond by entrapment or polymeric adhesion, and also because each lead wire is typically connected to the substrate only at one or two positions, making it easy to dislodge the sensors from their cavities by stresses applied to their lead wires. As a result, systems that
30 employ more than five sensors on a substrate often can be

used only once before one or more of the sensors become loosened or dislodged.

The lead wires need to be sheathed to prevent them from shorting out by contact with one another, and also
5   to prevent them from chemically reacting with most substrates. However, currently available sheathing adds significant weight to the lead wires, and can contribute particulate contamination to high temperature process environments.

10   When the lead wires extend across the surface of the substrate, where the temperature is typically highest, they are subject to reaction with the surrounding environment. Thus, the environment within which a particular structure can function without damage is
15   limited by the resistance of the lead wire material to reaction with and penetration by the surrounding environment. For example, type K TC wire is stable above 500°C only in inert and hydrogen environments, while type S TC wire is stable above 700°C only in inert and
20   oxidizing atmospheres. Furthermore, none of these lead wires are stable in reactive process gas environments.

The Al_2O_3/SiO_2 mixtures used for bonding the sensors to the substrate tend to yield only glazes, and generally do not react aggressively with most oxidizable surfaces
25   such as silicon of gallium arsenide wafers. The bond securing the sensor to the substrate tends to be relatively weak.

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SUMMARY OF THE INVENTION

The object of the present invention is to provide a packaging system capable of securely holding a body to a substrate at elevated temperatures, and encapsulating the body and associated lead wires to protect them from harmful environments. While applicable in general to generic bodies intended to be exposed to high temperatures (of at least about 460°C) when mounted on an oxidizable substrate, the invention is particularly useful in securing temperature and other environmental sensors and their associated lead wires to a semiconductor wafer.

A reacted borosilicate mixture (RBM) at least partially encapsulates the body and secures it relative to the substrate by means of an oxide interface formed between the RBM and substrate during the high temperature reaction process. The body can be non-oxidizable, in which case it is entrapped by the RBM and secured to the substrate by an oxide interface between the RBM and the substrate adjacent to the body. If the body is itself oxidizable, an oxide interface is also formed between the RBM and the body that provides additional bonding strength.

The RBM can either extend over a body which is in direct contact with the substrate, or the body can be completely encapsulated by the RBM. In the case of a thermal sensor in which the RBM is provided under as well as over the sensor, the RBM layer under the sensor is thin enough to provide a thermally conductive path between the substrate and sensor. The RBM is preferably a mixture of B_2O_3 and SiO_2, with the B_2O_3 content a function

of the reaction temperature and the desired bonding strength and viscosity.

Lead wires for environmental sensors can also be secured to the substrate by encapsulating the wires in RBM along at least a portion of their lengths. The RBM electrically insulates the lead wires from each other, thus eliminating the need for wire sheathing. It also facilitates the provision of multiple lead wires in either a single common level relative to the substrate, or in a multi-layer bundle. An array of multiple sensors and associated lead wires can be secured to a common substrate by the RBM, with the lead wires connected to an output facility.

Further features and advantages of the invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of an array of environmental sensors and associated lead wires distributed on a common substrate;

FIG. 2 is a sectional view of an oxidizable sensor chip completely encapsulated and bonded to a substrate by an RBM;

FIG. 3 is a sectional view of a non-oxidizable sensor chip encapsulated relative to a substrate by an overlying RBM;

FIG. 4 is a sectional view of a partially encapsulated sensor bonded to a substrate by an RBM;

FIGS. 5 and 6 are sectional views of a single layer of lead wires and a multi-layer lead wire bundle, respectively, bonded to a substrate and insulated from each other by an RBM;

5   FIG. 7 is a sectional view of a process temperature instrumented wafer bonded to a cap wafer by an RBM;

FIG. 8 is a graph of the thermal coefficient of expansion for SiO_2-B_2O_3 RBM as a function of the relative quantity of each constituent; and

10   FIG. 9 is a flow diagram illustrating a method of securing a body to a substrate in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

15   FIG. 1 illustrates one embodiment of the invention, in which an array of environmental sensors 2 are distributed over the surface of a substrate such as a semiconductor wafer 4 to detect a desired environmental parameter such as temperature, radiation, pressure, gas

20   composition or gas concentration. While the term "substrate" refers to a semiconductor wafer in FIG. 1, the term is not intended to be limited to this type of structure, and in general encompasses any type of body to which another body can be secured as described below.

25   The sensors are electrically connected by respective lead wires 6 which extend along the wafer surface to an output facility 8, such as visual readout indicators for the various sensors. Each lead wire 6 shown in FIG. 1 represents a plurality of lead wires, normally 2,3 or 4,

30   depending upon the type of sensor. The lead wires 6 can either be brought off the wafer individually or assembled

into a bundle 10 which, for the 17 sensor system illustrated, preferably organizes the lead wires in a multi-layer stack. When multiple sensors are employed, the lead wires can be connected to a terminal block 12,

5   which can be either on or off the wafer, with output wires 14 from the terminal block connecting the lead wire to the output facility 8. An input stimulus or energization can also be applied to the sensors through appropriate lead wires.

10   While 17 sensors are shown, this is for purposes of illustration only; greater or smaller numbers of sensors could also be employed. The lead wire paths and the location of the lead wire bundle 10, as well as the number of lead wire bundles, are matters of design

15   choice. While a circular substrate is shown, the substrate can be of any desired shape or size.

       One way to secure the sensors to the substrate is illustrated in FIG. 2. In this example the sensor is provided as an AlN chip 16 which carries a SiC sensing

20   element (not shown). This type of sensor is described in PCT Patent Application No. PCT/US00/07557 by the present inventor, published November 30, 2000, the contents of which are hereby incorporated by reference. The sensor is secured to the wafer 4 by means of a reacted borosilicate

25   mixture (RBM) of SiO_2 and B_2O_3. The RBM illustrated in FIG. 2 is applied in two steps: a first layer 18 on the wafer surface that underlies the chip 16 and extends along the wafer lateral to the chip, and a second layer 20 that overlies the chip and extends over the first RBM

30   layer lateral to the chip. The composition and processing of the RBM are described in

detail below. The first RBM layer 18 chemically bonds with the wafer 4 by forming a thin oxide interface 22, typically not more than 1,000 Angstroms thick. This RBM layer chemically and electrically isolates the chip 16

5 from the wafer, but is thin enough to permit efficient transfer of heat from the substrate to the wafer in the case of a temperature sensor.

Both RBM layers 18 and 20 chemically bond with the chip 16 by forming an oxide interface 24 with the chip

10 during reaction of the RBM. Where it extends onto the wafer surface beyond the limits of lower RBM layer 18, the upper RBM layer 20 also forms an oxide interface with the wafer during the reaction process to extend the RBM-wafer oxide interface 22. A thicker oxide interface is

15 formed with a wafer made from Si, GaAs or the like than with an AlN chip, which is less oxidizable than these wafer materials. Thus, only a small portion of wafer material, insufficient to effect its sensing capability, is consumed.

20 The arrangement illustrated in FIG. 2 is suitable for TC junctions. If desired to enhance heat transfer from the wafer, the TC junctions can be disposed within cavities in the wafer and secured by RBM layers as shown.

The oxide interfaces firmly secure the chip to the

25 wafer. The chip retention is considerably stronger than prior epoxy and bonding techniques. Although for some temperature sensors it may be desirable to place the sensor within a cavity in the wafer for greater heat transfer, cavities are not required for mechanical

30 adhesion of either the sensors or their lead wires, and for this purpose can be eliminated entirely.

While the RBM oxidizes a small portion of the chip 16, it effectively encapsulates the chip and protects it from more extensive oxidation that it would otherwise suffer in an oxidizing environment at elevated
5   temperatures. Highly oxidizable materials such as tungsten might be completely oxidized by the environment when heated, but are protected by the RBM and lose only a small portion of their mass to oxidation during the thermal reaction process used to form the RBM.

10   Another embodiment of the invention is illustrated in FIG. 3. In this case the sensor chip 16a is formed from a non-oxidizable material such as gold or platinum. The chip 16a is placed directly in contact with the wafer 4 and coated with a single RBM layer 26, which extends
15   onto the wafer lateral to the chip. When reacted, the RBM lateral to the chip forms a thin oxide interface 28 with the wafer, but no oxide is formed with the chip. In this case the chip is entrapped by the RBM, which securely holds it to the wafer via the RBM/wafer oxide interface
20   28, and protects it from the environment.

While the invention thus far has been described in terms of an environmental sensor secured to an underlying wafer, it is applicable in general to securing any type of body to an oxidizable substrate. If the body itself is
25   oxidizable, the RBM chemically bonds with both the body and the substrate to produce a very strong adhesion mechanism. If only the substrate is oxidizable, the body is held on by entrapment, which is generally not as strong as bonding to both the substrate and body but is
30   still considerably stronger than prior epoxy or SiO_2-Al_2O_3 bonding.

FIG. 4 illustrates another embodiment in which it is desired to expose a sensor chip 16b to the environment, for purposes such as environmental gas or radiation sensing. In this case the RBM 30 extends from the surface
5 of substrate 4 over the edge of chip 16b and onto the upper surface of the chip a sufficient distance to securely hold the chip to the substrate. However, the RBM terminates short of the center of the chip, leaving a portion of the chip surface 32 exposed to the
10 environment. The RBM forms a retaining oxide interface 34 with the substrate when it is reacted, and also forms an oxide interface with the chip if the chip is made of an oxidizable material. No such chip-RBM oxide interface is shown in FIG. 4, for the case of a non-oxidizable chip.

15   In addition to holding a sensor chip or other body onto a substrate, the RBM is also preferably employed to retain lead wires associated with the sensor on the substrate. This is illustrated in FIG. 5 for the case of a single layer, 4-wire bundle of lead wires 36. The lead
20 wires are spaced from each other and fully encapsulated in an RBM 38, which forms an oxide interface 40 with the underlying substrate 4 when the RBM is reacted. The RBM both spaces and insulates the lead wires from each other, while securely retaining them relative to the substrate.
25 While the RBM is shown after it has been reacted, a form 42 that can be used to maintain the spacing between lead wires and hold the lead wires in place during the reaction process is shown in dashed lines. The form 42 includes downward directed knife-edge protrusions 44 that
30 extend around the upper portions of the lead wires for this purpose. The form is clamped in place over the RBM,

lead wires and substrate during the reaction process, and then removed.

A greater number of lead wires can conveniently be accommodated in a multi-layer bundle, as illustrated in
5   FIG. 6. Thirty-four lead wires 46 are illustrated, corresponding to two lead wires for each of the 17 sensors of FIG. 1; other types of sensors can employ different numbers of lead wires. The wires are arranged in four layers 48a, 48b, 48c and 48d. Each upper layer
10   preferably contains fewer lead wires and the layer immediately below, with the positions of the lead wires staggered from layer to layer for greater structural integrity. In the illustration of FIG. 6 the first, second, third and fourth lead wire layers from the bottom
15   of the bundle have 10, 9, 8 and 7 wires, respectively. All of the lead wires are spaced from each other and securely retained in place with respect to the substrate by a mass of RBM 50 that encapsulates at least a portion of the length of each lead wire, and is secured to the
20   substrate 4 by an oxide interface 52 formed with the substrate during reaction of the RBM.

In encapsulating the lead wires 46, the RBM 50 can eliminate the need for lead wire sheathing. This reduces the overall weight of the device and also avoids
25   particulate contamination at high temperatures that can occur with sheathing.

The RBM 50 may or may not chemically bond with the lead wires 46, depending upon whether the lead wires are or are not oxidizable. If a chemical bond with the lead
30   wires does occur, the resulting oxide interface will generally be less than 1,000 Angstroms thick, which will

still leave the bulk of the lead wires available for electrical conduction.

An RBM as described herein can be used in general to adhere any two or more oxidizable bodies to each other.
5   As an example, FIG. 7 illustrates a process temperature instrumented wafer (PTIW) 52 consisting of a semiconductor wafer 54 which bears a temperature sensor structure 56. The PTIW is capped by a second semiconductor wafer 58 which provides both mechanical and
10 radiation protection for the sensor, and strengthens the overall device. The two wafers 54 and 58 are adhered to each other by an RBM layer 60 that surrounds the sensor 56 on the opposed surfaces of both wafers. The RBM forms oxide interfaces 62 and 64 with the wafers 54 and 58,
15 respectively, when it is reacted at an elevated temperature, bonding the two wafers together. Heat is transferred through both wafers to the sensor. With or without sensors, two or more oxidizable wafers or other bodies can be adhered together through the RBM. The
20 wafers can be of either similar or dissimilar materials, such as Si-Si, GaAs-GaAs or GaAs-Si. If desired, the RBM could be extended to encapsulate all or a desired portion of the overall structure.

Borosilicate compositions have historically been
25 used for commercial glasses and glazes, such as crown glasses, flint glasses and pyrex glasses used to form beakers. However, they have not been used for high temperature retention purposes such as those proposed in the present application.
30 With a proper selection of RBM materials and fabrication technique, the RBM can be made to form an

environmental barrier over sensors, other bodies and their associated lead wires that would otherwise be susceptible to degradation in anticipated environments. The properly formed RBM protects the underlying materials from all vapor and liquid environments, except those such as HF which are known to etch SiO_2.

It has been discovered that, with an appropriate proportion of B_2O_3, an SiO_2-B_2O_3 RBM will form an environmental barrier over sensors such as TC junctions, Pt RTD chips and any lead wires that may be susceptible to environmental degradation, that such a RBM will accommodate mismatches in thermal expansion between the lead wires and sensors on one hand and the substrate to which they are attached during both slow and rapid thermal cycling for commonly used materials, and that the thermal energy required to form the RBM will not damage the sensors, lead wires or substrate. The RBM functions as an electrical insulator up to at least 1300°C, and is both chemically and mechanically stable at temperatures in excess of 1300°C. It also retains a strong adhesion to oxidizable materials, via the formation of an oxide interface during thermal reaction, for temperatures of at least 1200°C.

Some important properties of B_2O_3 and SiO_2 for this purpose are:

-       A crystalline form melting temperature of 460°C for B_2O_3 and 1610°C for SiO_2.

-       A glass softening temperature of 1665°C for SiO_2.

- Both materials are excellent electrical insulators, and form a continuous substitutional glass mixture.

5   - The thermal coefficient of expansion (TCE) of the RBM can be matched to particular sensor and substrate materials by an appropriate selection of the SiO_2-B_2O_3 mix ratio.

- They can be mixed together and applied to surfaces as dry powders, permitting both surface and bulk
10   reaction to occur simultaneously. They can also be applied as a paste, but the paste should be dried before being reacted to avoid spitting.

- Crystalline form molecular weights of 69.62 grams/mole for B_2O_3 and 60.08 grams/mole for SiO_2.

15

The TCE for the RBM is plotted as a function of the SiO_2-B_2O_3 average coordination number in FIG. 8. The "average coordination number" is a measure of the mole percentages of SiO_2 and B_2O_3 in the RBM in which 3.0
20   corresponds to 100% B_2O_3 and 4.0 corresponds to 100% SiO_2, with intermediate average coordination numbers being a linear function of the relative mole percentages. It can be seen that the TCE increases generally exponentially with increasing percentages of B_2O_3.

25   Typical ceramic substrates include, but are not limited to, Al_2O_3, alumina-silicates, alumina-boro-silicates, AlN, BeO, B_4C, BN, C, leachable-ceramics, glass-ceramics, mica, SiO_2 (glass and crystal), SiC, Si_3N_4, SrO, TiB_2, TiO_x, $(WC)_{94}$ Co_6, Y_2O_3, magnesia-
30   stabilized Z_rO_2, yttria-stabilized Z_rO_2, and Z_rO_2. Typical semiconductor substrates include, but are not limited to,

Ge, Si, Ga As, InP, InSb, InAs, CdTe, CdInTe, HgCdTe, and SiC.

In general, the TCE of lead wires will be substantially greater than that of substrates, except for metallic substrates. For example, a type-K TC is comprised of a 90wt%Ni/10wt%Cr wire and a 95wt%Ni/5wt%AlSi wire. The TCE of each wire is approximately that of Ni, or about $16 \times 10^{-6}/°K$ at 500°C. The TCE of Si is about $4.1 \times 10^{-6}/°K$ at 500°C. This suggests that the RBM will need to accommodate significant expansion mismatches between the substrate and the wires during thermal cycling. Thus, the preferred RBM should have a low softening temperature so that it can absorb the expansion mismatch and "heal" itself during rapid thermal cycling. This calls for an RBM with greater than $70wt\%B_2O_3$.

The starting B_2O_3 and SiO_2 materials for the RBM can be powder, grains or crystals. For adhesive and/or entrapment applications, the B_2O_3 and SiO_2 are preferably ground separately and then mixed; for environmental barrier applications, the B_2O_3 and SiO_2 are preferably first mixed together, and the mixture ground into a fine powder. In both cases the average post grinding particle size should be less than 500 microns, the smaller the better. It can be applied to the sensor and substrate surfaces as a dry powder or dispersed in an organic solvent, which should be dried before reacting to prevent spitting.

A reaction takes place when the B_2O_3/SiO_2 mixture and the components upon which it is placed are heated to at least 460°C, preferably in an oxidizing or alternatively

in an inert (Ar or N_2) atmosphere. The reaction temperature should not exceed 1300°C. Heating can be accomplished by conventional and rapid thermal techniques. The reaction proceeds most favorably when the components are passed through the melting temperature of B_2O_3 as rapidly as possible. The preferred heating technique is anticipated to be rapid thermal annealing using IR heating.

In general, higher reaction temperatures will tend to produce a more vigorous reaction. This reduces the chance of residual unreacted B_2O_3 being left after the reaction in case the SiO_2 and B_2O_3 have not been mixed well enough or they have not been ground to a sufficiently small particle size. Also, higher reaction temperatures encourage the formation of a RBM glass that completely encapsulates a body over which the RBM has been applied, rather than a glaze. For lower reaction temperatures, the proportion of B_2O_3 in the mix should be increased to retain good adhesion characteristics between the RBM and the bodies it adheres together.

The reaction temperature will often be limited by the thermal capability of the materials with which the RBM is used. For example, GaAs should generally not be heated to more than about 900°C, while a silicon substrate bearing a device structure should not be heated to more than about 1,100°C, and then only for very short periods of time.

Factors other than the reaction temperature that can affect the relative proportions of SiO_2 and B_2O_3 in the mixture include the desired bonding strength and viscosity of the RBM. Lowering the proportion of B_2O_3

increases the RBM's viscosity, resulting in a higher bonding strength. On the other hand, a higher viscosity means the RBM has a lower TCE and does not flow as easily. This makes it less able to tolerate bonding to

5 combinations of materials having significant TCE differences when operated over a temperature range that produces serious expansion mismatches between the materials. In general, the selection of the SiO_2/B_2O_3 ratio will involve a balancing among the reaction

10 temperature and the desired bonding strength and viscosity.

One fabrication technique for mounting a sensor to a wafer substrate is illustrated in FIG. 9. This can be used to form the structure illustrated in FIG. 2. In the

15 first step 66, the wafer is masked to expose only those areas for which RBM is desired. Alternately, RBM could be applied over the entire wafer, especially if the wafer is devoted exclusively to sensors and their associated lead wires. In the next step 68, a layer of the desired

20 borosilicate mixture (BM) is applied to the exposed wafer surface if a mask is used, or over the entire wafer surface if there is no mask. This BM layer should have a thickness (within the range of about 0.1 mm – 10 mm, with the lower end of the range preferred for a thermal sensor

25 to avoid significant interference with heat transfer from the wafer to the sensor.

In the next step 70 the sensor and its lead wires are laid down over the unreacted BM layer so that the lead wires extend from the sensor to beyond the edge of

30 the wafer (or to any terminal block that may be provided on the wafer). A second layer of unreacted BM powder (wet

or dry) is then applied over the sensor, lead wires and first BM layer in step 72, followed by clamping a form such as that shown in FIG. 5 over the lead wires to space the wires from each other and hold the wires and the
5   sensor against the first unreacted BM layer (step 74).

    The assembly is then placed in an oven or furnace and heated to at least 500°C for at least 15 seconds, with a thermal ramp that passes through the 460°C B_2O_3 melting temperature as rapidly as possible (step 76).
10   This causes the BM to cure and chemically bond with any underlying oxidizable surfaces via a thin oxide layer, thus forming a strong mechanical attachment of the RBM to the material with which it has bonded. The procedure for the first sensor is completed in step 78 by removing the
15   form, and inspecting and qualifying the part.

    Multiple sensors can be mounted to the wafer simultaneously by this method, as long as their lead wires are brought off of the wafer in a single layer. If multi-layer lead wire bundles are desired, all of the
20   sensors having lead wires in the lowermost layer can be mounted simultaneously as described, followed by removal of the mask. A new mask is then applied to expose the RBM over the first lead wire layer, and also the areas on the wafer that will be occupied by the next set of sensors
25   and their associated lead wires. The second layer of lead wires will extend over the wafer surface from their associated sensors until they reach the first lead wire layer, at which point they cross over to the top of the RBM covering the first lead wire layer as illustrated in
30   FIG. 6. The second set of sensors and lead wires are then coated with another BM layer, and the unreacted BM is

cured as before. The process is repeated for each subsequent lead wire layer and its associated sensors, as indicated by step 80.

The invention has been successfully demonstrated by
5   several tests in which various types of chips were mounted onto ceramic and semiconductor surfaces.

Test 1

AlN chips which carried SiC temperature sensors were
10   mounted to Si wafers using RBM as described above, with a
B_2O_3 wt.% of 50 to 75. The resulting structures were inserted into an atmospheric tube furnace at 600°C, 800°C, 1000°C and 1200°C. In each test the structures were left in the furnace for five minutes, then removed
15   from the furnace and placed on a cold metal plate, with a maximum time between removal from the furnace and placement on the plate of thirty seconds. The chips remained bonded to the wafers in all cases. However, except for the 600°C test, the wafers cracked from
20   thermal shock when placed on the cold plate.

Test 2

The same type of chips as in Test 1 were mounted onto GaAs wafers using RBM as described. The resulting
25   structures were inserted into an inert atmosphere in a tube furnace, and heated and cooled as in Test 1 (except no test was performed at 1200°C, which is above the GaAs melting temperature). All of the chips remained bonded to the GaAs wafers, and all GaAs wafers cracked from thermal
30   shock when placed on the cold plate.

Test 3

Al$_2$O$_3$ ceramic chips were mounted onto Si wafers using SiO$_2$-B$_2$O$_3$ RBM to emulate the surface mounting of platinum TFRTDs, and tested as in Test 1. The chips remained
5   bonded to the wafers in all cases when the B$_2$O$_3$ wt.% in the RBM was at least 75%, but did not adhere at lower percentages. Except for the 600°C test, all of the wafers cracked from thermal shock when placed on the cold plate.

10   ### Test 4

The Test 1 procedure was performed for small Si, GaAs, SiC and AlN chips mounted on Al$_2$O$_3$ ceramic dies with RBM. The chips remained bonded to the dies in all cases when the B$_2$O$_3$ wt.% in the RBM was at least 75%, but did
15   not adhere for lower percentages. All dies cracked from thermal shock when placed on the cold plate.

Test 5

Si, GaAs, SiC, Al$_2$O$_3$ and AlN chips were mounted onto
20   pyrolytic-boron-nitride (PBN) dies using RBM, and tested as in Test 1. The chips remained bonded to the ceramic dies in all cases when the B$_2$O$_3$ wt.% was at least 70% except for Al$_2$O$_3$, which required the B$_2$O$_3$ wt.% to be at least 75%.

25

Test 6

Si, GaAs, SiC, Al$_2$O$_3$, PBN and AlN chips were mounted onto graphite using RBM and tested as in Test 1. The results were the same as for Test 5.

30

Test 7

Si, GaAs, SiC, Al_2O_3, PBN, AlN and graphite chips were mounted on fused quartz (SiO_2 glass) using RBM, and tested as in Test 1. The chips remained bonded to the fused quartz in all cases when the B_2O_3 wt.% in the RBM

5   was at least 70% except for Al_2O_3, which required the B_2O_3 wt.% in the RBM to be at least 75%. All fused quartz (glass) substrates cracked when place on the cold plate.

10   Test 8

Si, GaAs, SiC, Al_2O_3 and AlN chips were mounted onto crystalline SiO_2 using RBM and tested as in Test 1. The results were the same as for Test 7.

15   The RBM was found to work best on non-oxide materials. In the case of oxides, specifically Al_2O_3 and SiO_2, the bond is not as strong as for non-oxide substrates. However, the bond to SiO_2 was stronger than to crystalline Al_2O_3.

20

Test 9

To test the high temperature thermal encapsulation capabilities of the RBM, thin films of tungsten metal, approximately 1000 Angstroms thick, were deposited on AlN

25   ceramic dies and partially coated with unreacted B_2O_3 + SiO_2 powder, with B_2O_3 wt.%s equal to and greater than 50%. The assemblies were then placed in an atmospheric tube furnace at 1000°C for five minutes, removed from the furnace, and allowed to cool in air. The tungsten not

30   coated by RBM was completely oxidized, as evidenced by a yellow color and electrical probing which showed it to be

an insulator. The RBM was etched from the coated portion of the tungsten with HF. The tungsten that had been coated was still intact, and its conductivity was unchanged from the value exhibited before coating and
5 heat treatment. Since tungsten oxidizes very readily in air, this test confirmed the ability of the RBM to protect metals from oxidizing during as well as after its formation, and strongly infers that the rate of reaction from a mixed powder to RBM is very rapid.

10 While several embodiments of the invention have been shown and described, numerous variations and alternate embodiments will occur to those skilled in the art. Accordingly, it is intended that the invention be limited only in terms of the appended claims.

15